REMARKS/ARGUMENTS

The present application provides a method, apparatus, and program product for a self-healing, reconfigurable logic emulation system, wherein if a signal wire becomes faulty in an emulation cable during an emulation run, runtime software on an externally connected host workstation can automatically reconfigure the emulator to reroute the data destined for the faulty signal wire across a spare wire. Such a feature enables a user to restart the emulation run without having to recompile the simulation model to account for the hardware fault.

Reconsideration of the application, as amended, is requested. Claims 1-8, 9, and 13 have been amended in this response, and no new matter has been added. Claims 1-16 remain pending in this application.

In section 8 of the 4/9/07 Final Office Action, the Examiner rejects claims 9, 10, 12-14, and 16 under 35 U.S.C. §102(b) as being anticipated by Yu, "Fault Tolerance in Adaptive Real-Time Computing Systems," a doctoral dissertation for Stanford University dated December 2001.

The Yu reference cited by the Examiner describes a real time computing system (e.g., fly-by-wire system, navigation system, etc.) where failures can result in data corruption and lower performance, leading to catastrophic failures (Yu, Abstract). Yu proposes several fault tolerant design techniques to be utilized within such real-time computing systems, such as the use of Field-Programmable Gate Arrays (FPGAs), to design more reliable real-time computing systems.

With respect to claims 9, 10, 12-14, and 16, the Examiner states that Yu discloses a method for the automatic reconfiguration of faulty signal wires in a logic simulation hardware emulator, the logic simulation hardware emulator having one or more source emulation processors coupled to one or more receiving emulation processors by a set of

emulation cables, each emulation cable having a plurality of signal wires; the plurality of signal wires comprising a plurality of regular signal wires and one or more predefined spare signal wires. The Examiner further states that the Applicants' assertion that Yu does not disclosure a "logic simulation hardware emulator" is not relevant, because the recitation occurs in the preamble.

In response, Applicants have amended independent claims 9 and 13 to now remove "logic simulation hardware emulator" from the preamble of the claim. The preamble of the claim now refers to an "emulation system", as shown in Fig. 1A of the present invention, and as discussed on page 3, lines 10-21 of the present application. Applicants submit that the "emulation system" 10 is only a part of the total apparatus of the present invention, since the apparatus further includes a host workstation external to the emulation system itself which controls the simulation activities occurring on the emulation system, detects faults occurring within the emulation system, and reconfigures the emulation system such that any of the signal wires having a fault are reassigned to one or more predefined spare signal wires via a runtime control program residing on the host workstation. Support for these elements can be found on page 3, lines 23-30, page 11, lines 12-18, and page 11, line 26 to page 12 line 5.

Applicants have further amended the body of claims 9 and 13 to now more clearly define the interaction between the emulation system 10, the host workstation 12, the logic model 15 and the control program 20 during the automatic reconfiguration of the faulty signal wires. Applicants wish to stress that the control program 20 residing on the external host workstation 12 controls the entire simulation process, including the detection of faults within the emulation system 10, and the reconfiguration of the faulty signal wires to predefined signal wires.

In contrast to the present invention, Yu performs its detection and reconfiguration entirely within the real-time computer itself. As stated on page 49, second paragraph of Yu, "Repair controllers are embedded in each of the FPGAs to perform error monitoring,

fault diagnosis, and reconfiguration tasks. When a permanent fault occurs in one of the FPGAs and is detected, the repair controller in the FPGA reports the fault to the controller in the other FPGA. The other controller evokes fault diagnosis for reconfiguration". See also Yu, Figure 6-1.

Thus, while Yu relies on the FPGAs themselves (i.e., the emulation processors) to perform fault detection and reconfiguration, the present invention relies on a control program residing on a host workstation external to the emulation system itself to detect faults within the emulation system, and reconfigure the system in the event of a fault.

Applicants respectfully submit that claims 9 and 13, as amended, now clearly distinguish the present invention over the cited Yu reference, and now place the claims in condition for allowance. Further, Applicants respectfully submit that dependent claims 10, 12, 14, and 16 rely, either directly or indirectly, from claims 9 and 13, which for reasons stated above, are now considered allowable. Thus, Applicants submit that claims 10, 12, 14, and 16 are also now in condition for allowance.

In section 10 of the Office Action, the Examiner rejects claims 1-6, 11, and 15 under 35 U.S.C. §103(a) as being unpatentable over Yu, "Fault Tolerance in Adaptive Real-Time Computing Systems," a doctoral dissertation for Stanford University dated December 2001, in view of Babb et al., "Logic Emulation with Virtual Wires," published in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol., 16, No. 6, June 1997.

In response, Applicants have amended independent claim 1 to now remove "logic simulation hardware emulator" from the preamble of the claim. The preamble of the claim now refers simply to an "apparatus". Within the body of the claim, the apparatus is further defined as having an emulation system (Fig 1A, element 10) coupled to a host workstation (Fig. 1A, element 12) via an interface cable, wherein a runtime control program 20 residing on the host workstation controls the simulation of a logic model 14

on the emulation system 10. More specifically, the runtime control program 20, upon detection of a fault on a signal wire within the emulation system 10, reassigns the faulty signal wire to the one or more spare signal wires.

Applicants submit that the "emulation system" 10 is only a part of the total apparatus of the present invention, since the apparatus further includes a host workstation external to the emulation system itself which controls the simulation activities occurring on the emulation system, detects faults occurring within the emulation system, and reconfigures the emulation system such that any of the signal wires having a fault are reassigned to one or more predefined spare signal wires via a runtime control program residing on the host workstation. Support for these elements can be found on page 3, lines 23-30, page 11, lines 12-18, and page 11, line 26 to page 12 line 5.

Applicants have further amended the body of claim 1 to now more clearly define the interaction between the emulation system 10, the host workstation 12, the logic model 15 and the control program 20 during the automatic reconfiguration of the faulty signal wires. Applicants wish to stress that the control program 20 residing on the external host workstation 12 controls the entire simulation process, including the detection of faults within the emulation system 10, and the reconfiguration of the faulty signal wires to predefined signal wires.

In contrast to the present invention, Yu performs its detection and reconfiguration entirely within the real-time computer itself. As stated on page 49, second paragraph of Yu, "Repair controllers are embedded in each of the FPGAs to perform error monitoring, fault diagnosis, and reconfiguration tasks. When a permanent fault occurs in one of the FPGAs and is detected, the repair controller in the FPGA reports the fault to the controller in the other FPGA. The other controller evokes fault diagnosis for reconfiguration". See also Yu, Figure 6-1.

Thus, while Yu relies on the FPGAs themselves to perform fault detection and reconfiguration, the present invention relies on a control program residing on a host workstation external to the emulation system itself to detect faults within the emulation system, and reconfigure the system in the event of a fault.

With regard to Babb, Applicants respectfully submit that the Babb reference neither discloses nor suggests the use of spare signal wires in any context, much less the specific context of a control program residing on a host workstation external to the emulation system itself to detect faults within the signals of an emulation system, and reconfigure the system to utilize predefined spare signals within the emulation system in the event of a fault.

Since neither the Yu or Babb reference, alone or in combination, disclose or suggest the claimed matter of a runtime control program residing on an external host workstation coupled to the emulation system for controlling a simulation model, wherein upon detection of a fault on one of the regular signal wires, the runtime control program reassigns the signal on the regular signal wire having the fault to the one or more spare signal wires, Applicants respectfully submit that claim 1 should be passed to issuance.

Moreover, with regard to claim 1, the Examiner states that Yu discloses simulated square wave responses for systems on page 88-89 and Table 1, which implies that simulation is performed on the interconnected emulation processors. Applicants respectfully submit that what is disclosed on page 88-89 and in Table I of Yu, are results when the robot control system employed within the Yu real time computer was emulated by an external simulation system (i.e., Quickturn's System Realizer) in order to verify its functionality. The simulated square wave responses cited by the Examiner are actually generated by the external Cadence Quickturn emulation system, and are not in any way generated by the real-time computer system of Yu itself.

Also, with regard to claim 1, the Examiner states that Yu does not disclose expressly the emulation processors being embodied in a simulation model, or the runtime control program controlling the simulation model. The Examiner goes on to state that the emulation processors as disclosed in Yu are actually FPGAs and that Babb discloses the simulation of interconnected FPGA chips based on a simulation model.

While the Applicants agree with the Examiner that the Babb reference does indeed describe a logic simulation hardware emulator, Applicants submit that the real-time computer system described by Yu has nothing to do with logic simulation or hardware emulation, and in fact, Yu teaches away from simulation/emulation since systems such as Babb and the present invention are inherently not real-time (i.e., the simulators perform the simulation and speeds orders of magnitude less than the real time speed of the hardware being simulated/emulated). Thus, Applicants respectfully submit that there is no motivation to combine the non-real time simulator/emulator reference of Babb with the real-time computing system reference of Yu.

For these reasons, Applicants respectfully submit that claim 1 of the present invention is non-obvious with respect to Yu in light of Babb, and should be in condition for allowance.

Applicants further submit that claims 2-6 depend, either directly or indirectly, from claim 1, which for reasons stated above, is now submitted as being in condition for allowance. Thus, Applicants submit that claims 2-6 are also now in condition for allowance, and should be passed to issuance.

With regard to claim 11, Applicants respectfully submit that neither the Yu or Babb reference, alone or in combination, disclose or suggest the claimed matter of detecting a fault on one or more of the signal wires within the emulation system via a runtime control program residing on a host workstation externally coupled to the emulation system and reconfiguring the emulation system via the runtime control

program, wherein any of the signal wires having a fault are reassigned to one or more predefined spare signal wires (i.e., Yu performs the detection/reassignment within the real-time computer system itself, not via a runtime control program residing on an externally connected host workstation, and Babb does no detection/reassignment in any context). For these reasons, Applicants respectfully submit that claim 11 of the present invention is non-obvious with respect to Yu in light of Babb, and should be in condition for allowance.

With regard to claim 15, Applicants respectfully submit that neither the Yu or Babb reference, alone or in combination, disclose or suggest the claimed matter of detecting a fault on one or more of the signal wires within the emulation system via a runtime control program residing on a host workstation externally coupled to the emulation system and reconfiguring the emulation system via the runtime control program, wherein any of the signal wires having a fault are reassigned to one or more predefined spare signal wires (i.e., Yu performs the detection/reassignment within the real-time computer system itself, not via a runtime control program residing on an externally connected host workstation, and Babb does no detection/reassignment in any context). For these reasons, Applicants respectfully submit that claim 15 of the present invention is non-obvious with respect to Yu in light of Babb, and should be in condition for allowance.

In section 11 of the Office Action, the Examiner rejects claims 7-8 under 35 U.S.C. §103(a) as being unpatentable over Yu, "Fault Tolerance in Adaptive Real-Time Computing Systems," a doctoral dissertation for Stanford University dated December 2001, in view of Babb et al., "Logic Emulation with Virtual Wires," published in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol., 16, No. 6, June 1997, and further in view of Rush, US Patent No. 5,742,181. Applicants respectfully traverse this rejection.

With regard to Rush, Applicants respectfully submit that the Rush reference neither discloses nor suggests the use of spare signal wires in any context, much less the specific context of a control program residing on a host workstation external to the emulation system itself to detect faults within the signals of an emulation system, and reconfigure the system to utilize predefined spare signals within the emulation system in the event of a fault, as provided by claim 1, which claims 7-8 depend from.

Since none of the Yu, Babb, or Rush references, alone or in combination, disclose or suggest the claimed matter of a runtime control program residing on an external host workstation coupled to the emulation system for controlling a simulation model, wherein upon detection of a fault on one of the regular signal wires, the runtime control program reassigns the signal on the regular signal wire having the fault to the one or more spare signal wires, Applicants respectfully submit that claims 7-8 should be passed to issuance.

In view of the foregoing comments and amendments, the Applicants respectfully submit that all of the pending claims (i.e., claims 1-16) are in condition for allowance and that the application should be passed to issue. The Examiner is urged to call the undersigned at the below-listed telephone number if, in the Examiner's opinion, such a phone conference would expedite or aid in the prosecution of this application.

CERTIFICATE OF ELECTRONIC TRANSMISSION

I hereby certify that this correspondence and any enclosures are being electronically transmitted via EFS-WEB on the date indicated below.

August 31, 2007
(Date)
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